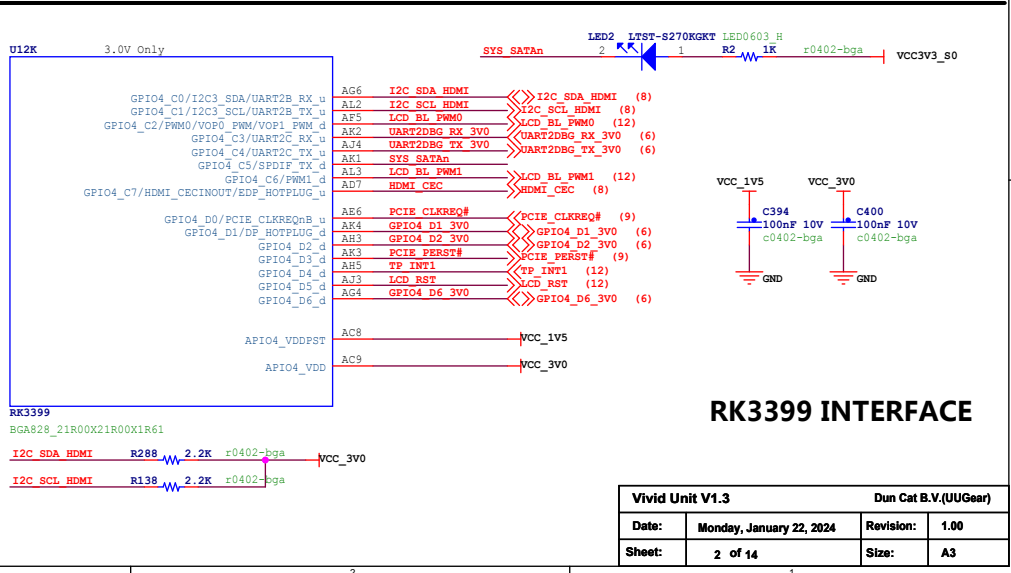
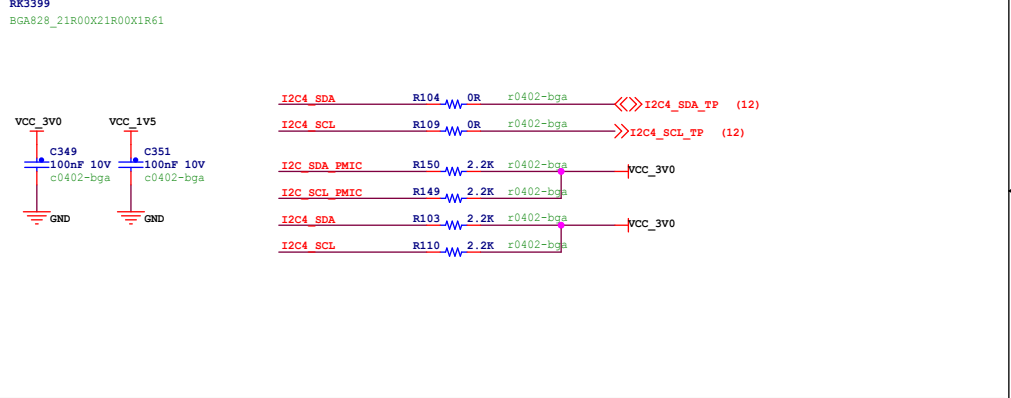
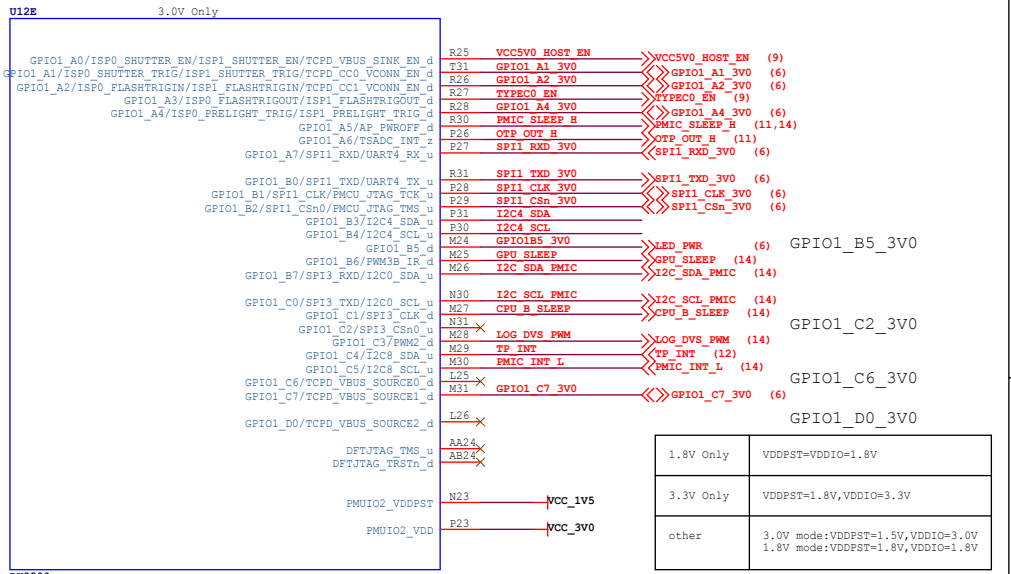
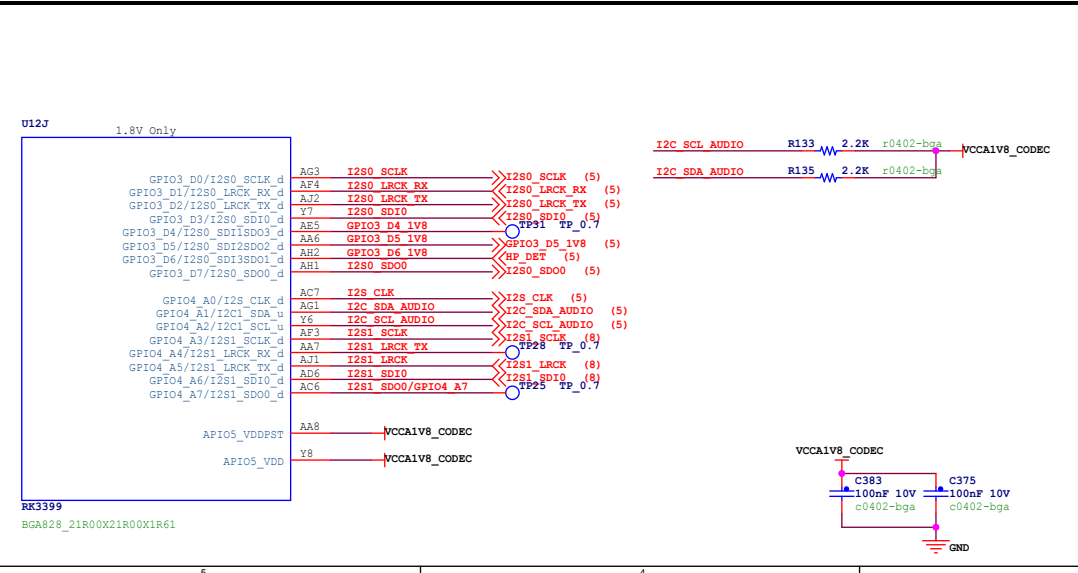
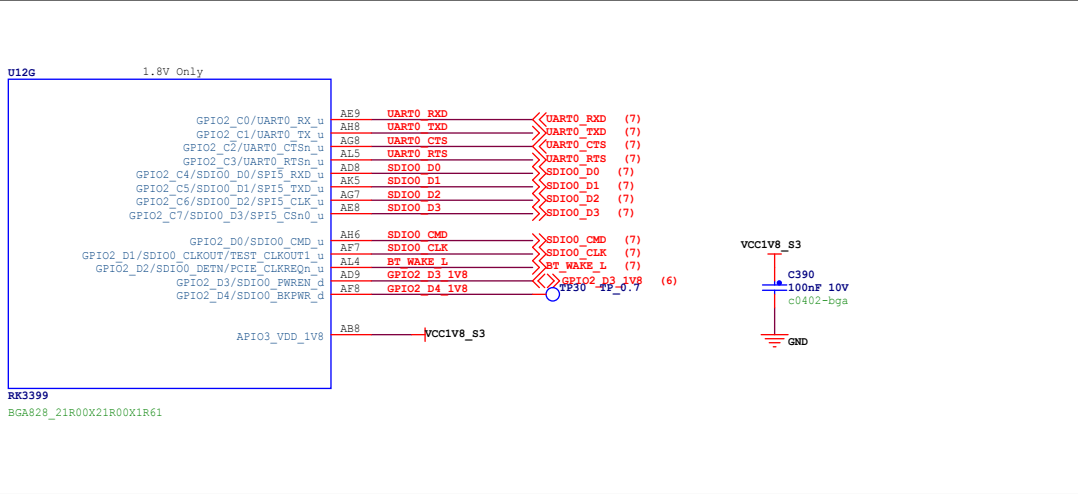
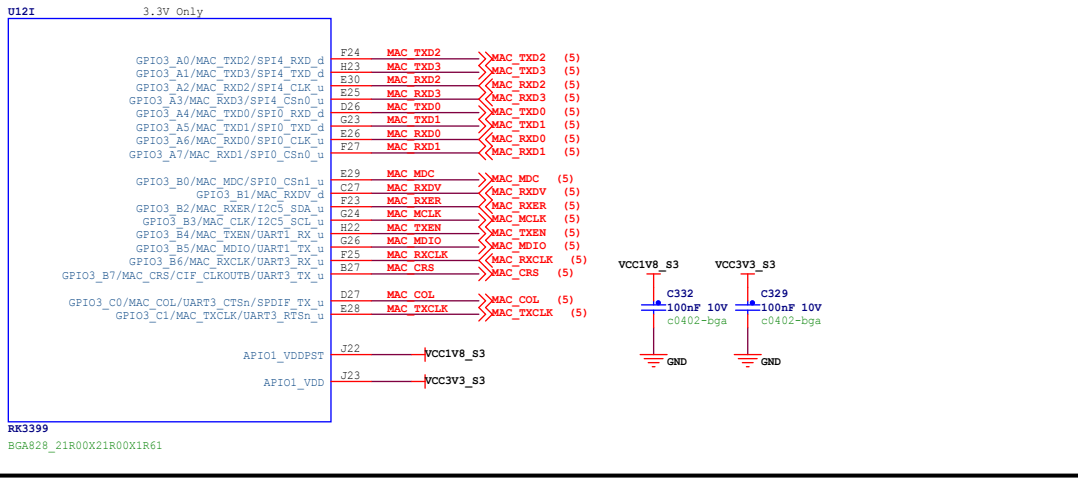


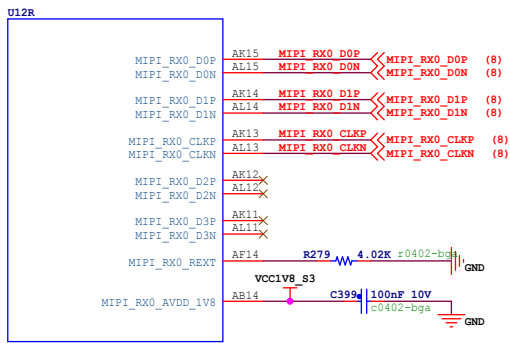
PAGE NO.	SCHEMATIC PAGE
1	COVER PAGE
2	RK3399 INTERFACE
3	RK3399 CTRL MIPI CSI DSI EDP
4	RK3399 PCIE USB SD EMMC ADC
5	RK3399 NET AUDIO
6	40 GPIO
7	BT WIFI KEY
8	HDMI MIPI POE MIC FLASH
9	USB 3.0 SSD
10	RK3399 DDR CTRL
11	RAM-LPDDR3-1
12	RAM-LPDDR3-2
13	RK3399 POWER
14	PMU-RK808-D

REV	Description	DATE	BY
Rev 1.0	Production release.	22/12/2022	Wanytech

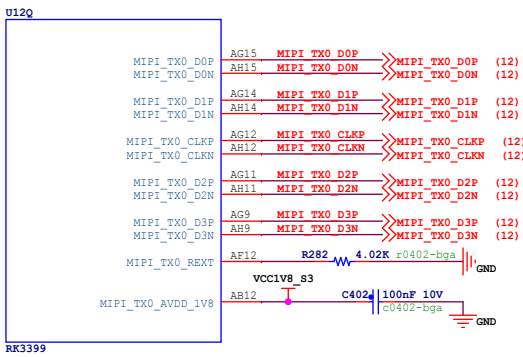


**RK3399 INTERFACE**

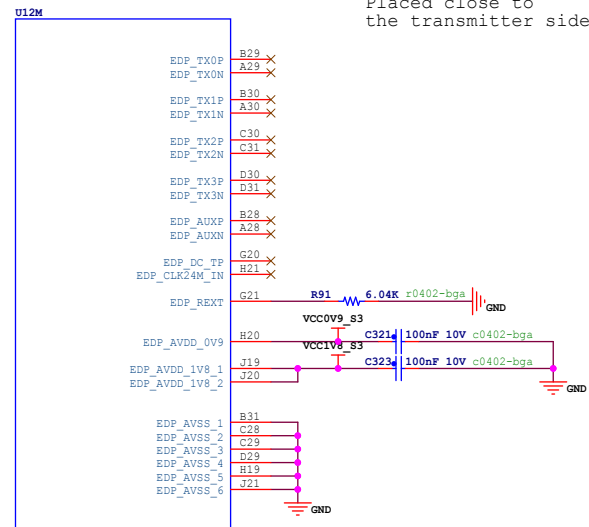
Vivid Unit V1.3		Dun Cat B.V.(UUGear)	
Date:	Monday, January 22, 2024	Revision:	1.00
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RK3399  
BGA828\_21R00X21R00X1R61

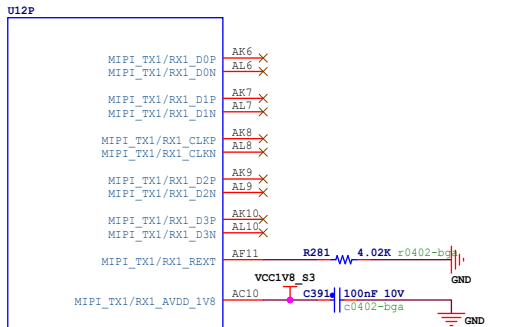


RK3399  
BGA828\_21R00X21R00X1R61

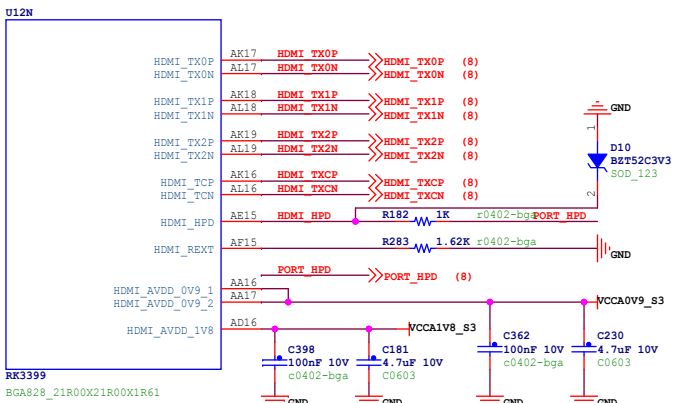


RK3399  
BGA828\_21R00X21R00X1R61

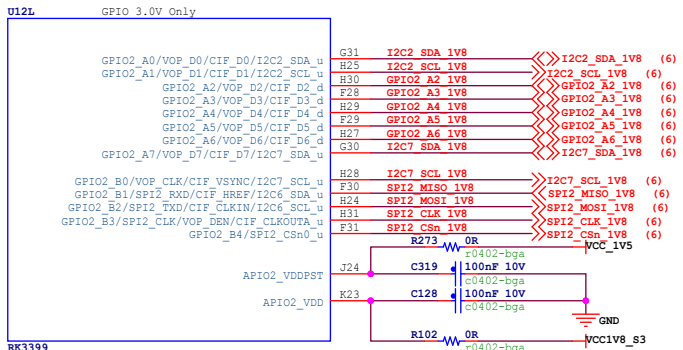
Placed close to the transmitter side



RK3399  
BGA828\_21R00X21R00X1R61

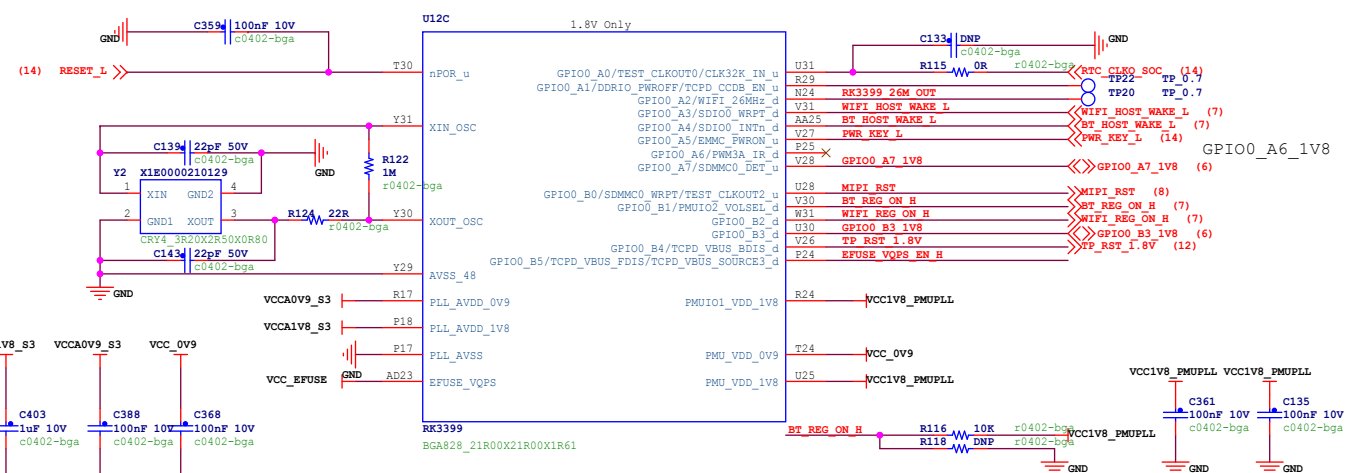


RK3399  
BGA828\_21R00X21R00X1R61



RK3399  
BGA828\_21R00X21R00X1R61

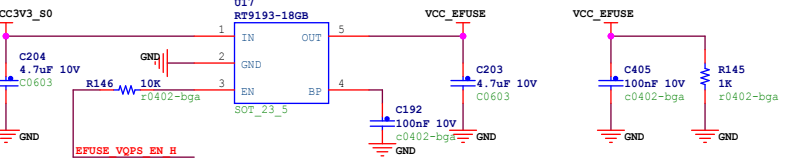
func1	func2	func3
GPIO2_A0/CIF_B0		I2C2_SDA
GPIO2_A1/CIF_B1		I2C2_SCL
GPIO2_A7/CIF_D7		I2C7_SDA
GPIO2_B0/CIF_VSYNC		I2C7_SCL
GPIO2_B1/CIF_HREF	SPI2_RXD	I2C6_SDA
GPIO2_B2/CIF_CLKI	SPI2_TXD	I2C6_SCL
GPIO2_B3/CIF_CLKO	SPI2_CLK	
GPIO2_B4/DVP_FPDN_H	SPI2_CS#	



RK3399  
BGA828\_21R00X21R00X1R61

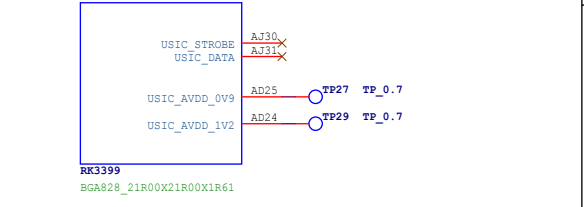
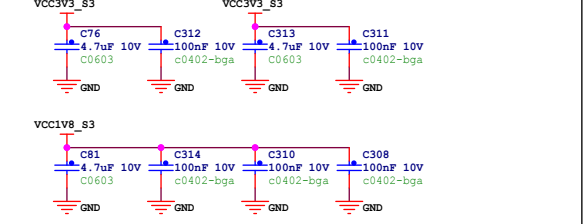
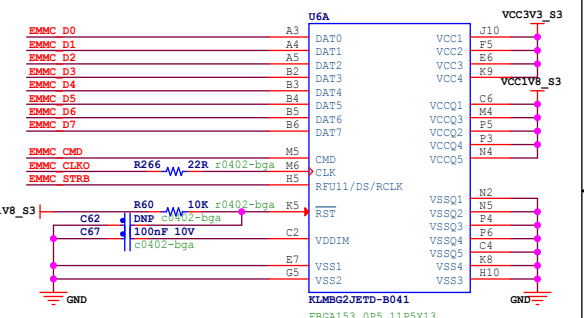
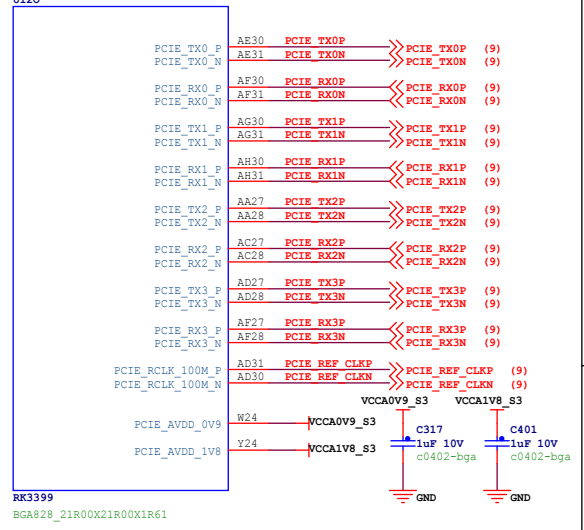
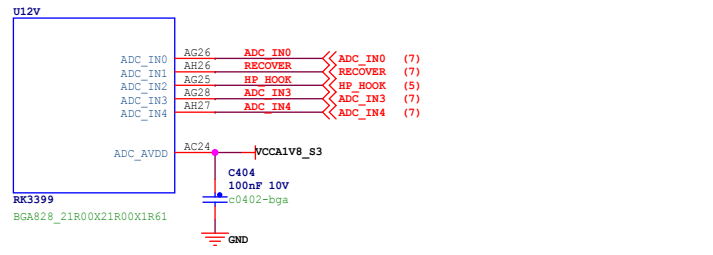
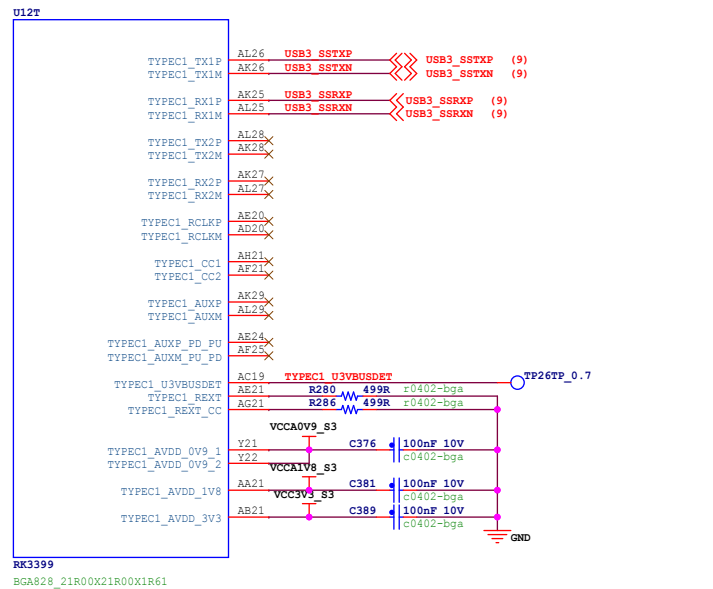
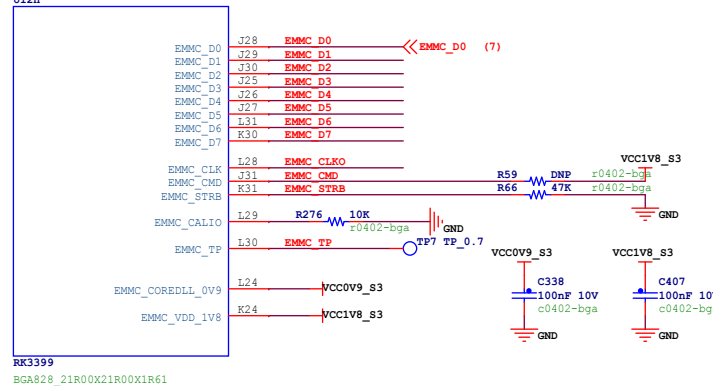
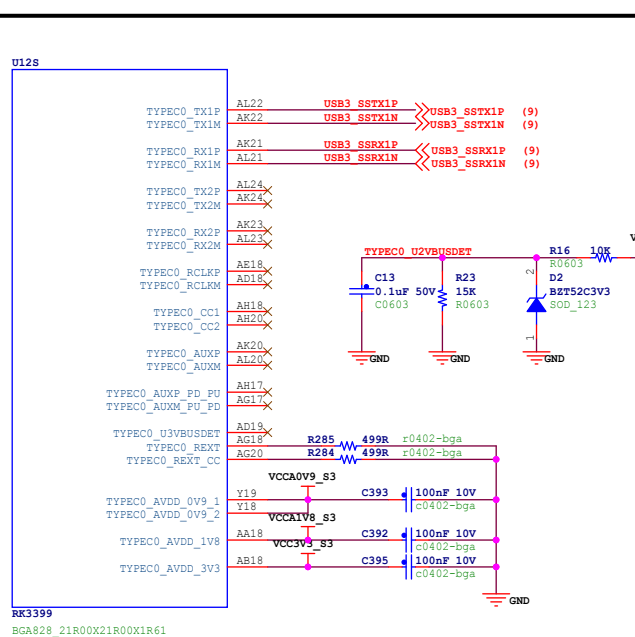
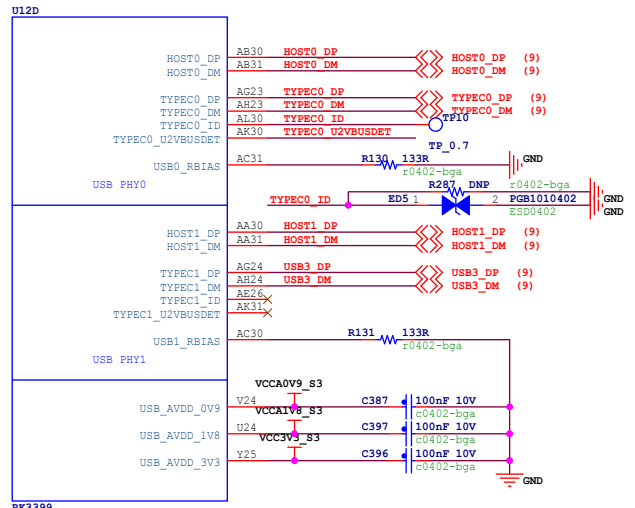
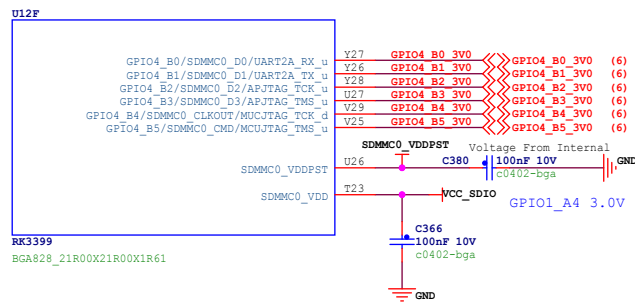
1.8V@0.3A

### RK3399 MIPI CSI DSI CIF EDP AND CONTROL



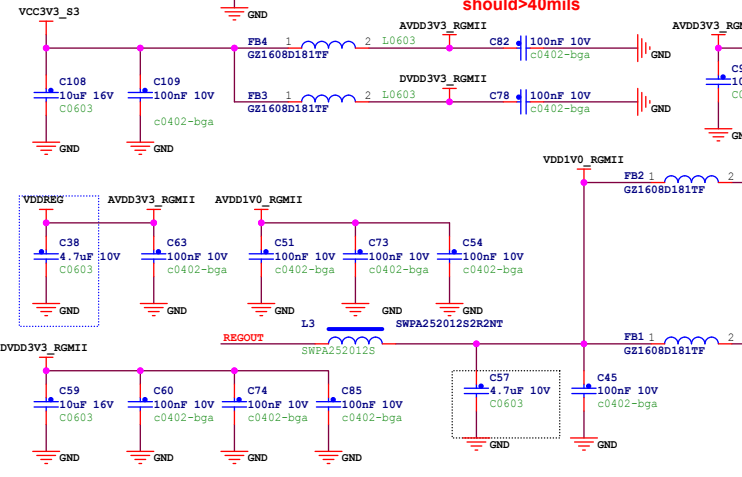
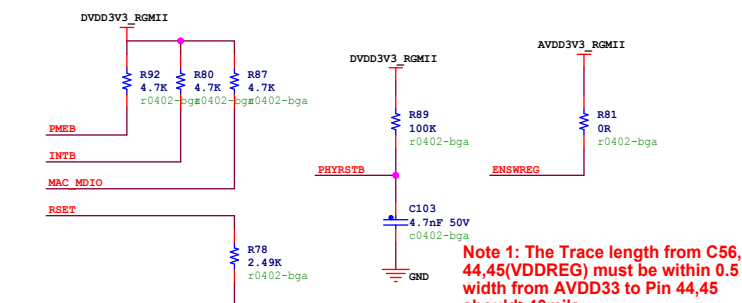
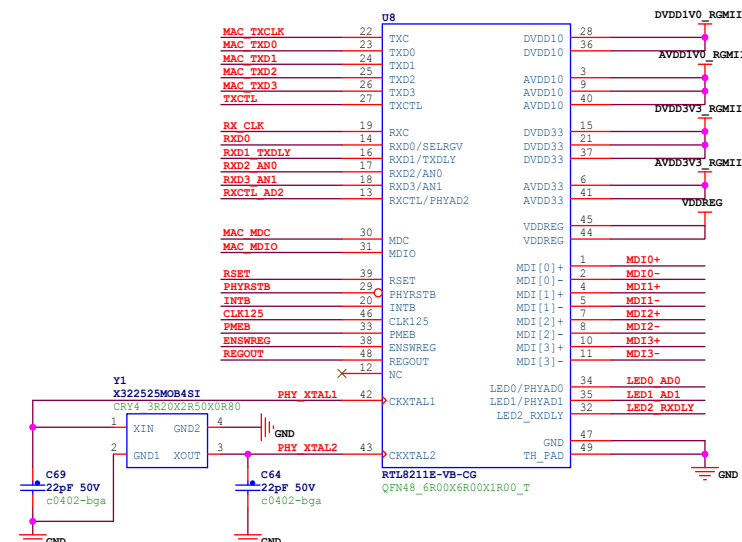
RK3399  
BGA828\_21R00X21R00X1R61

Vivid Unit V1.3		Dun Cat B.V.(UUGear)	
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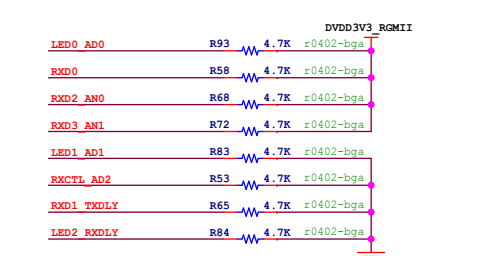


### RK3399 USB EMMC SD ADC

<b>Vivid Unit V1.3</b>		<b>Dun Cat B.V.(UUGear)</b>	
<b>Date:</b>	Monday, January 22, 2024	<b>Revision:</b>	1.00
<b>Sheet:</b>	4 of 14	<b>Size:</b>	A3



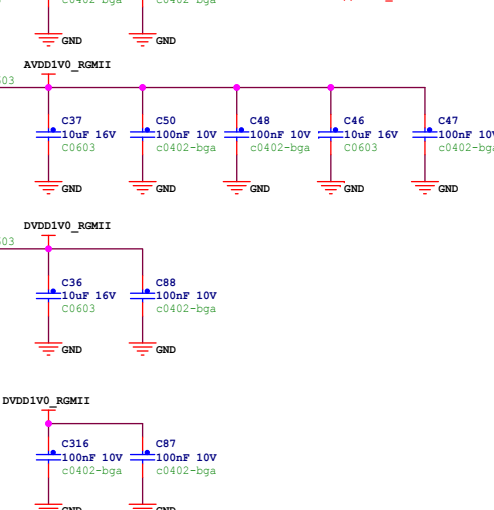
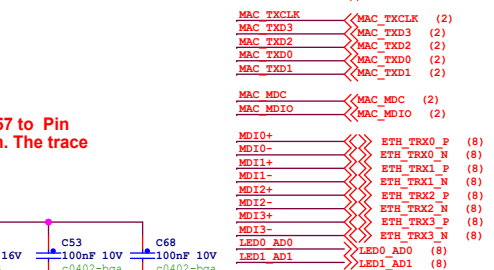
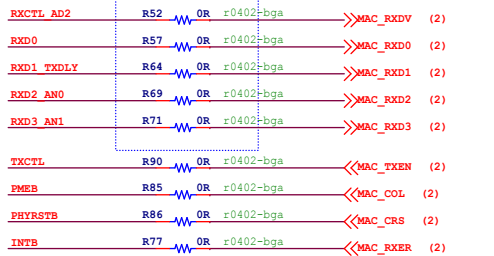
**Note 2:** The Trace length between L1 and PHY's Pin48 must be within 0.5cm. C35 and C36 to L1 must be within 0.5cm. Any inductance or bead except for L1 is not allowed on the path from REGOUT to DVDD10/AVDD10.



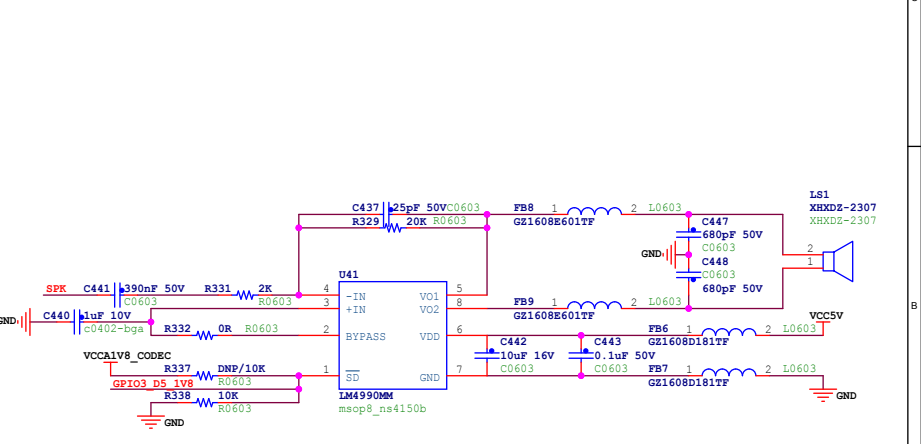
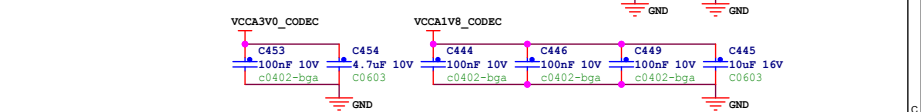
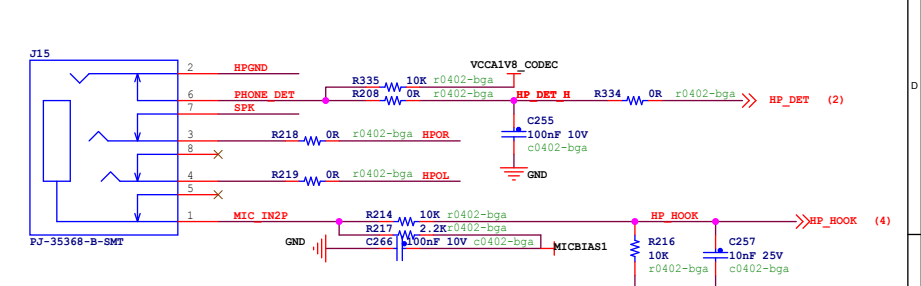
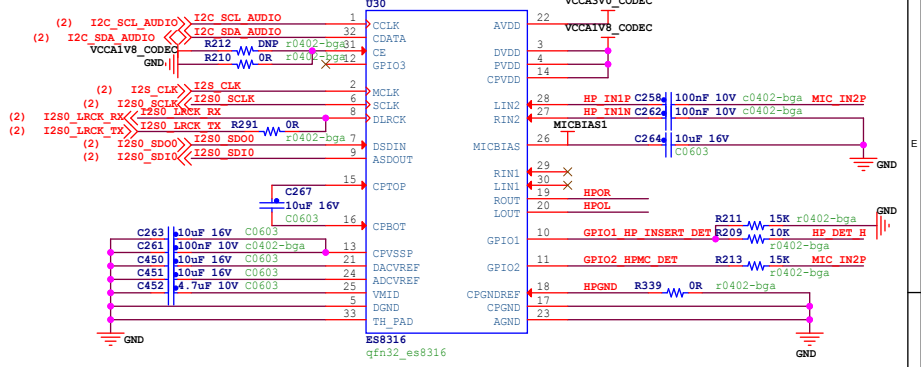
**R61,R62:** Config for all capability  
**R51,R54,R148:** PHY Address=001(RTL8211E)  
**R64,R50:** Without TX/RX Delay



Place filter network close to RX\_CLK. Reserved for EMI



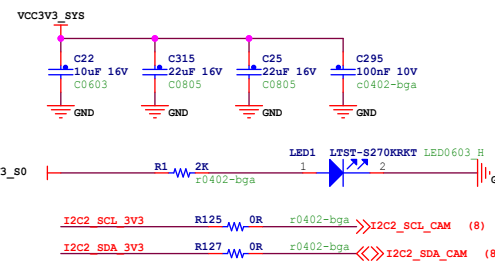
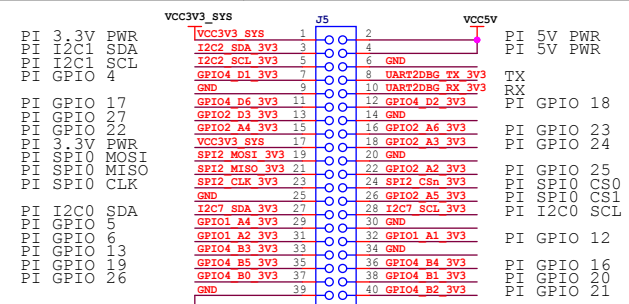
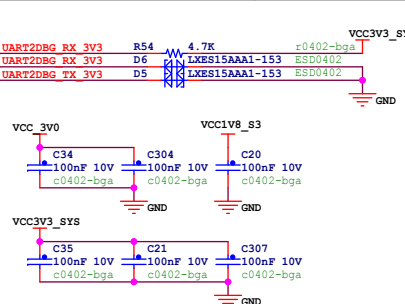
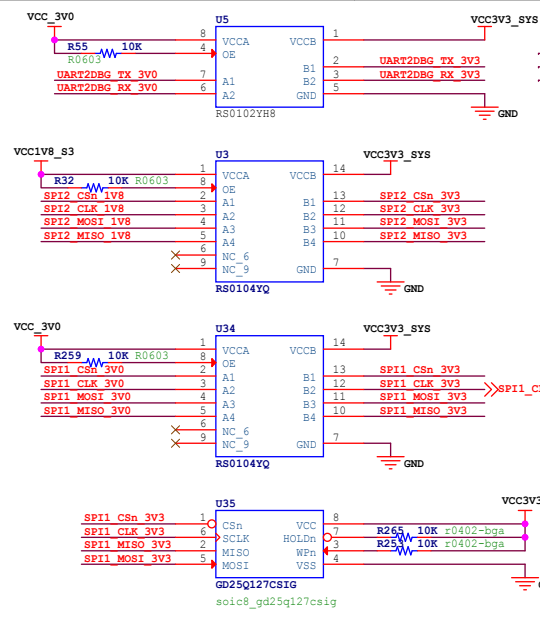
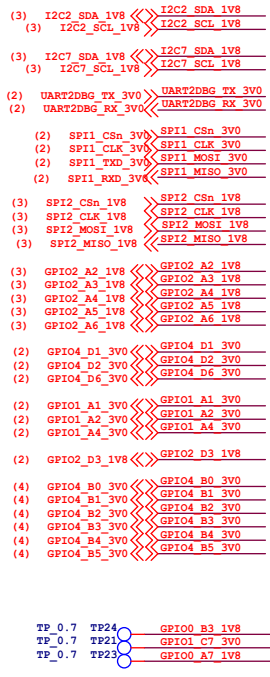
**RK3399 GBE**



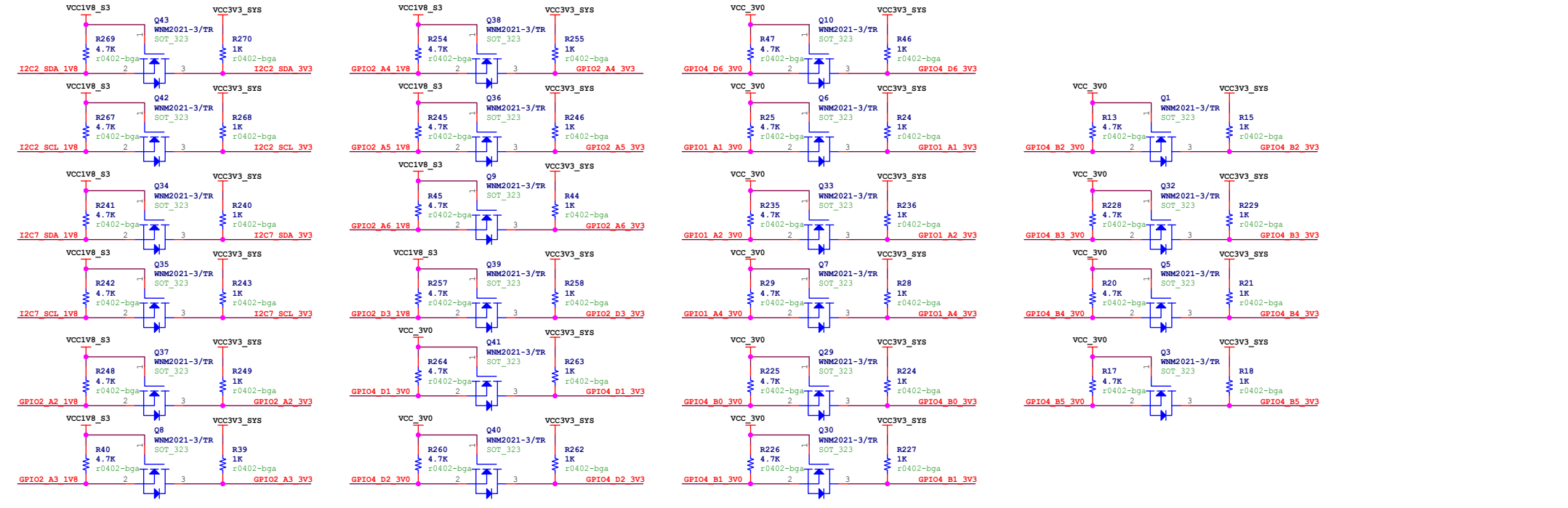
(2) GPIO3\_D5\_Iv8 >> GPIO3\_D5\_Iv8

**AUDIO INTERFACE**

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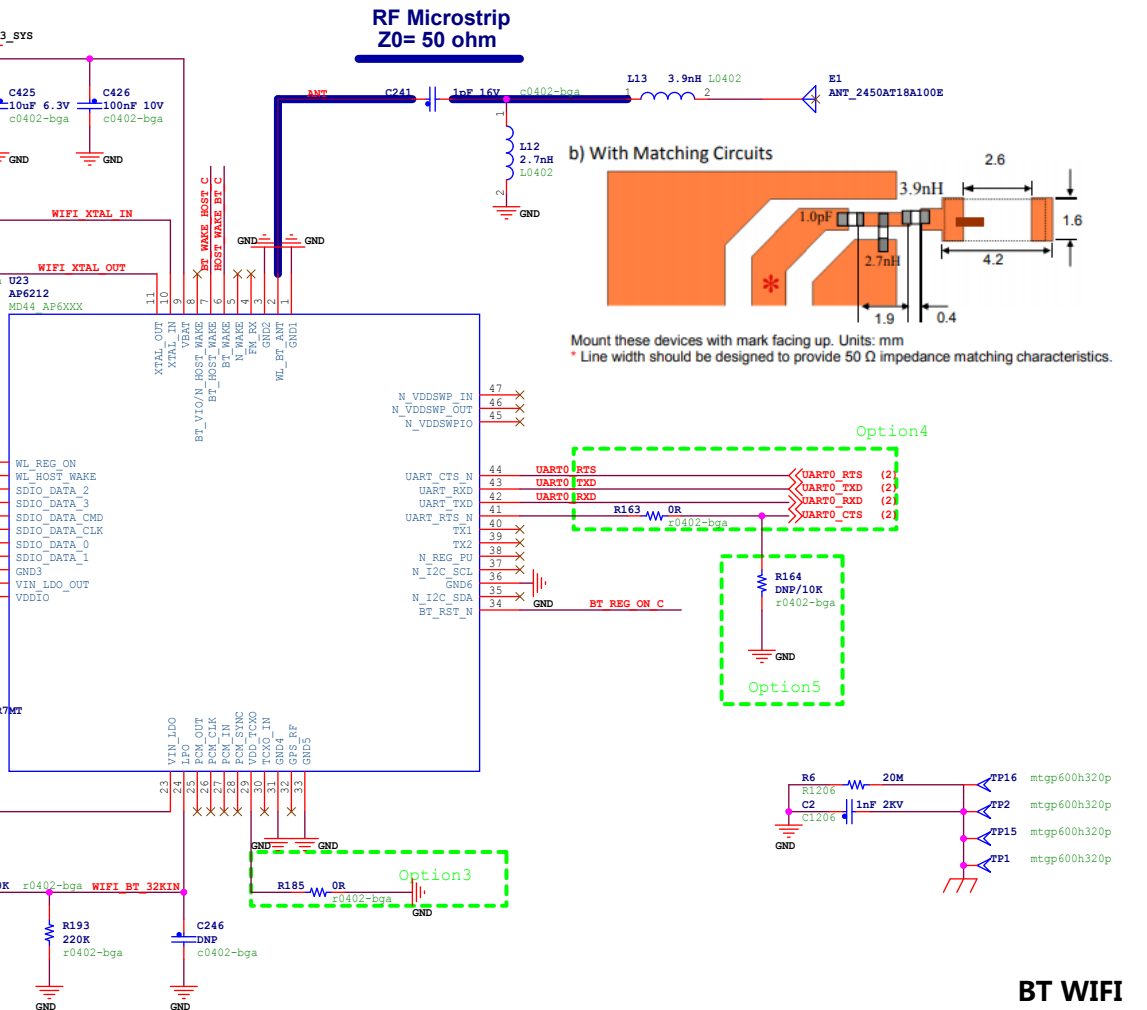
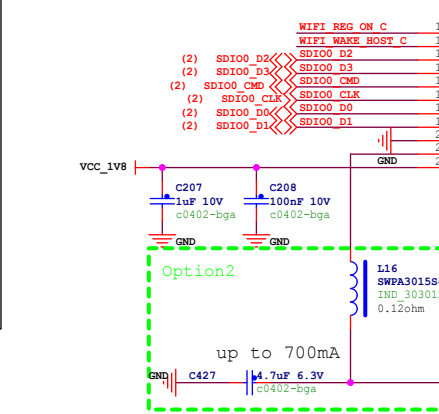
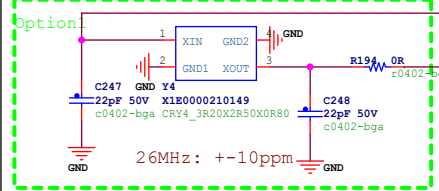
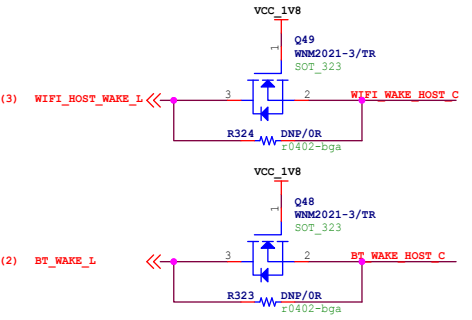
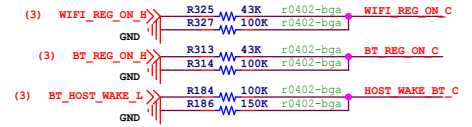
**Flash**



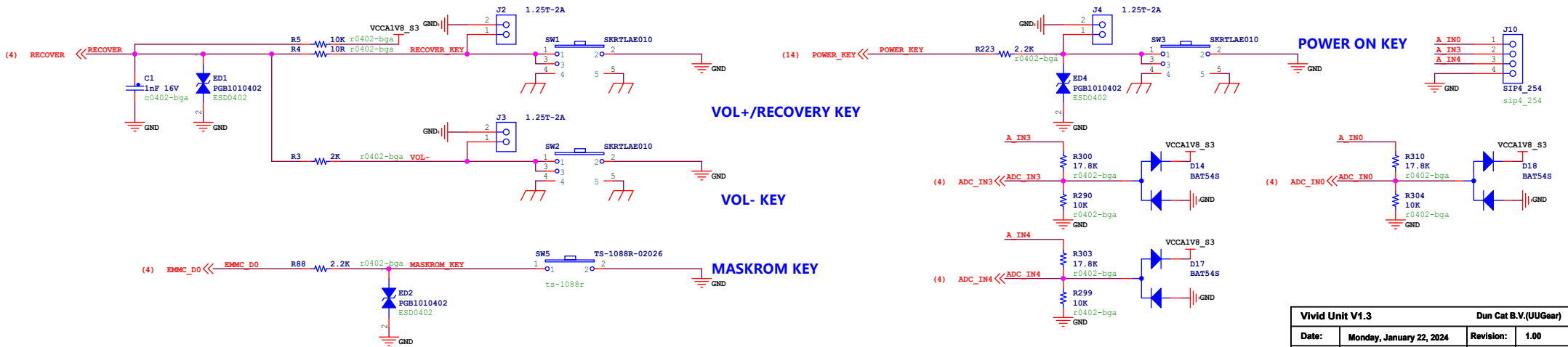
Vivid Unit V1.3		Dun Cat B.V.(UUGear)	
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# WIFI/BT Module

## Level Shift

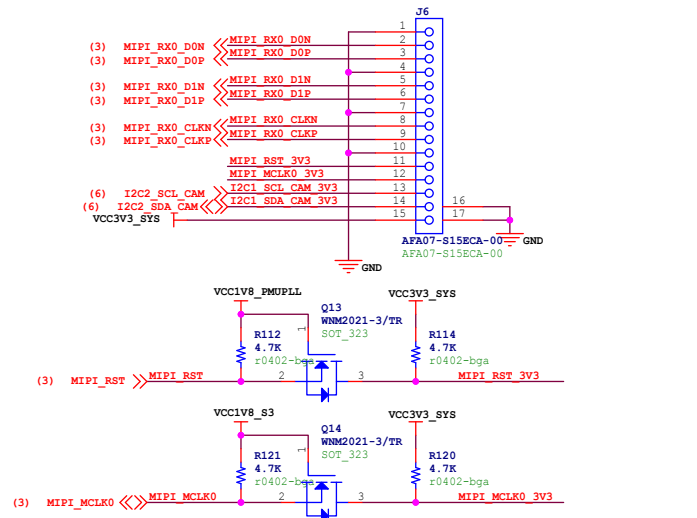


## BT WIFI

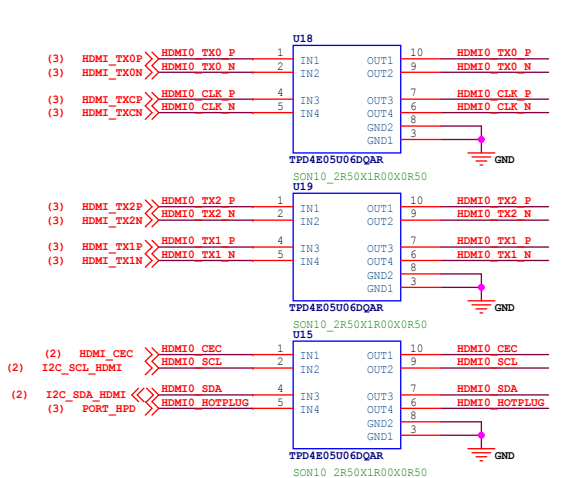


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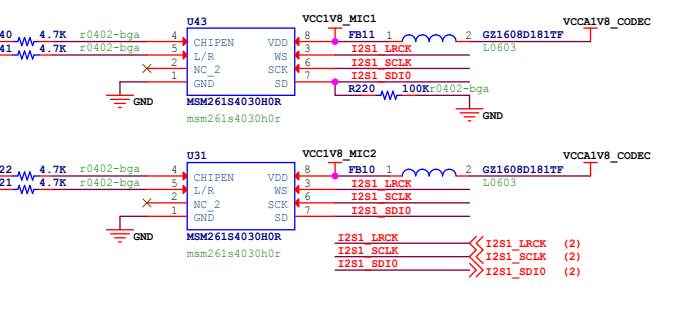
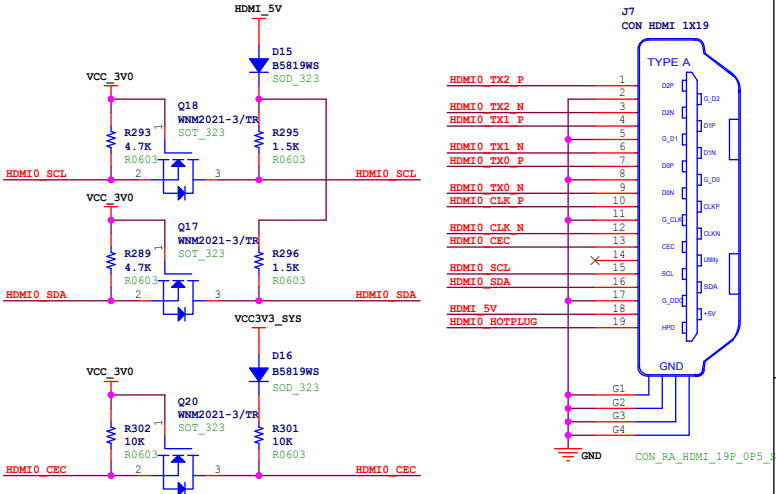




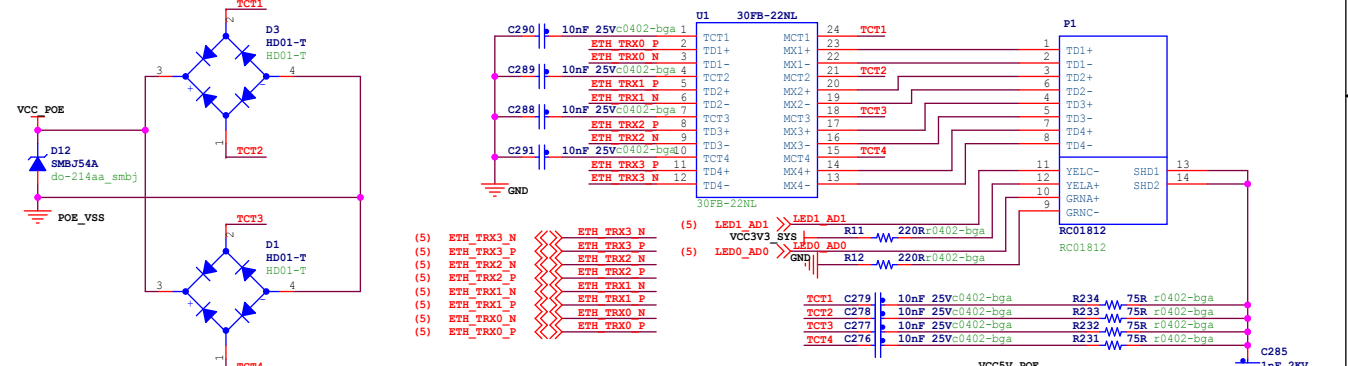
**CAMERA INTERFACE**



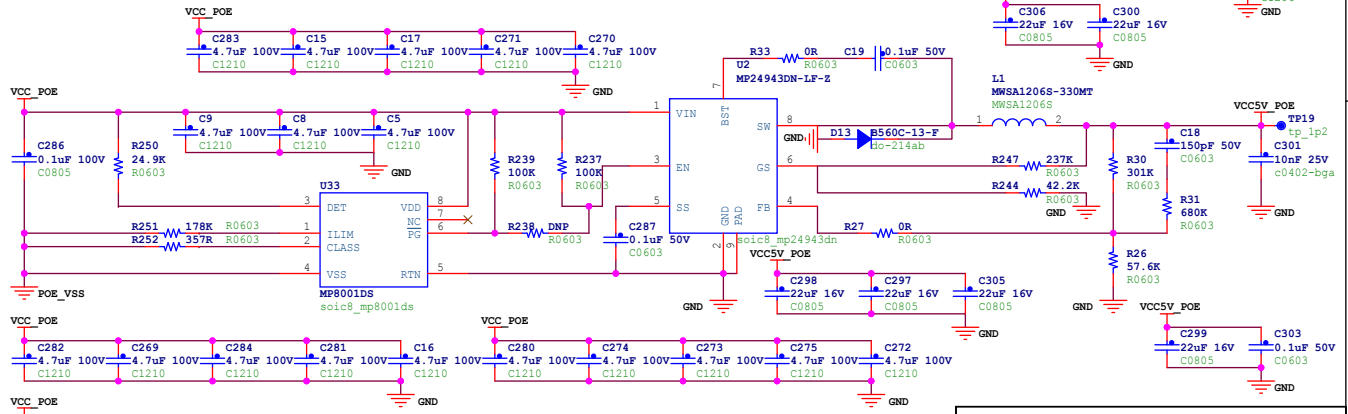
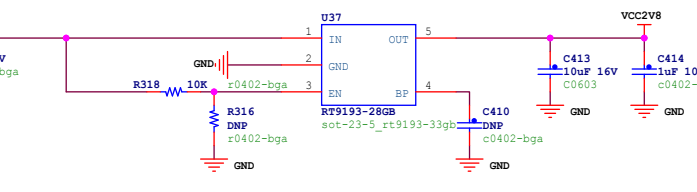
**HDMI**



**DIGITAL MICROPHONE**

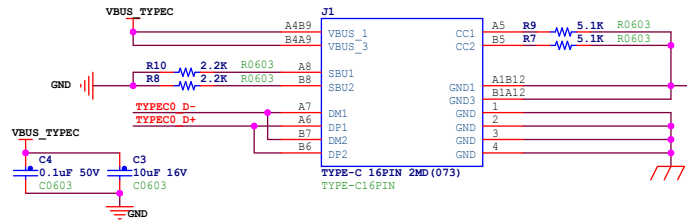
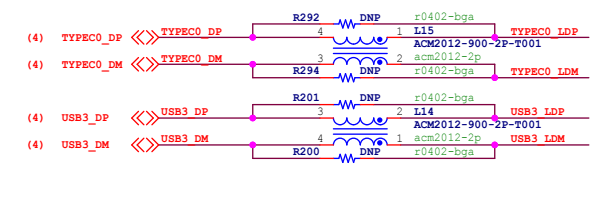


**POE**

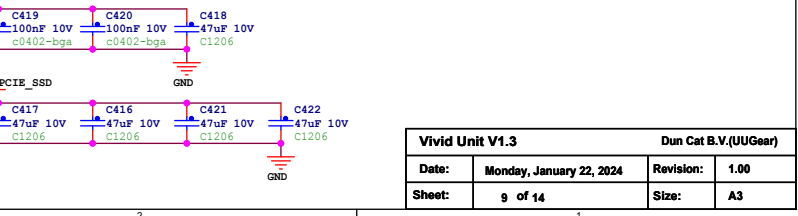
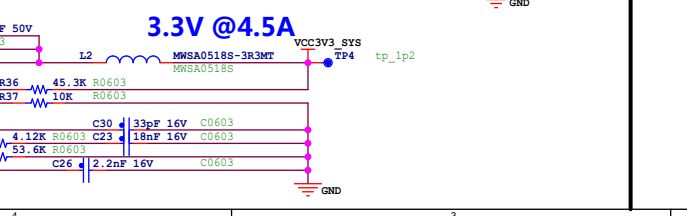
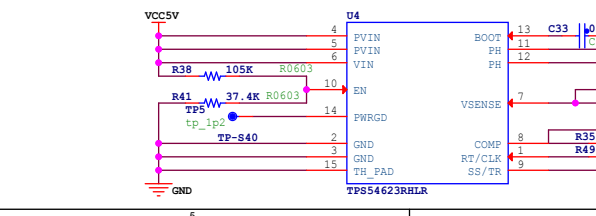
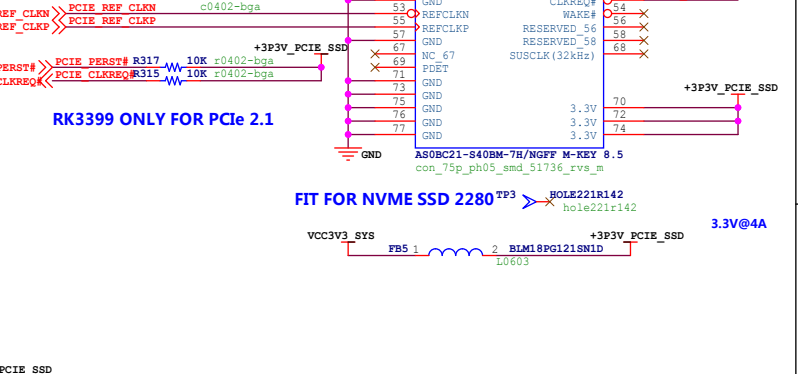
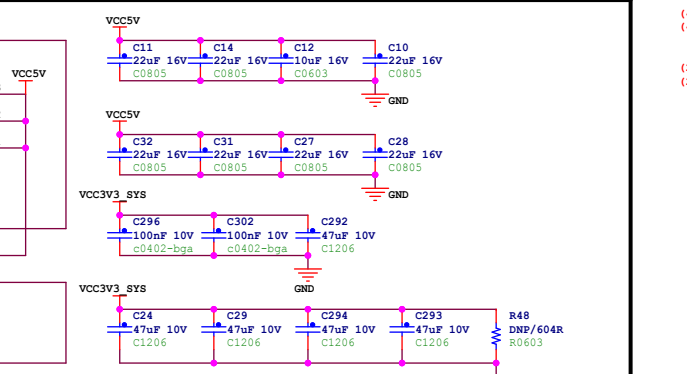
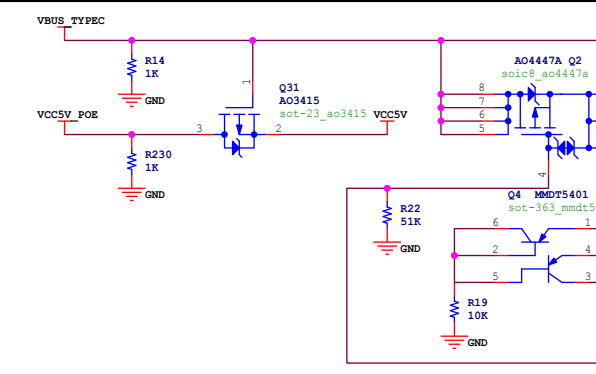
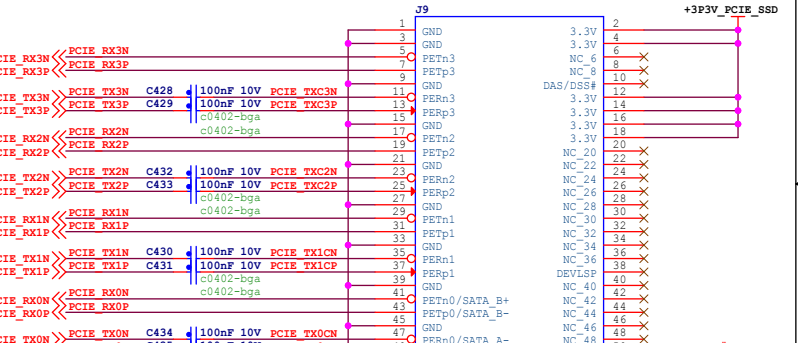
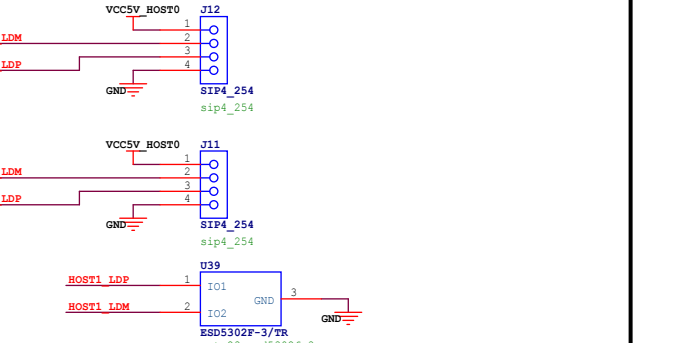
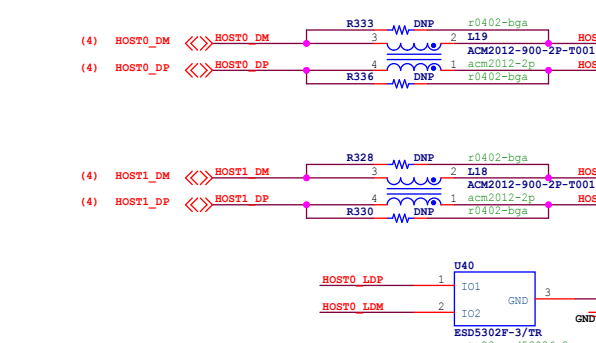
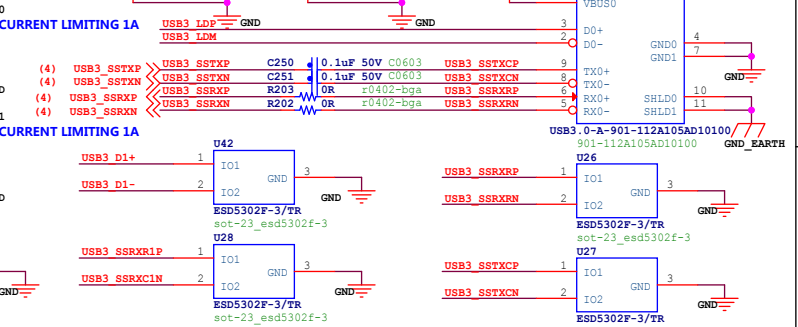
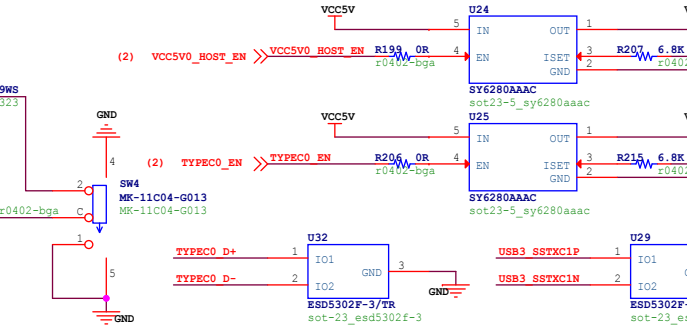
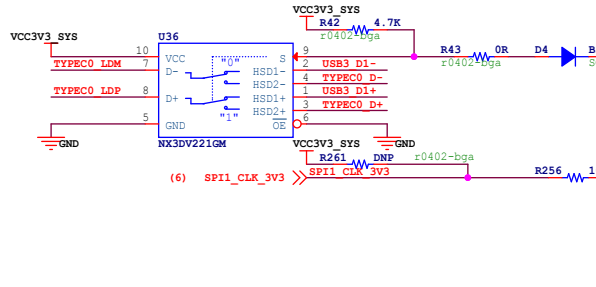
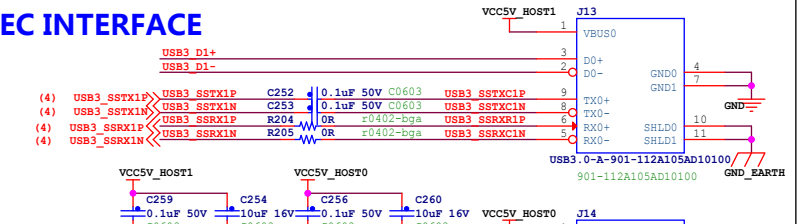


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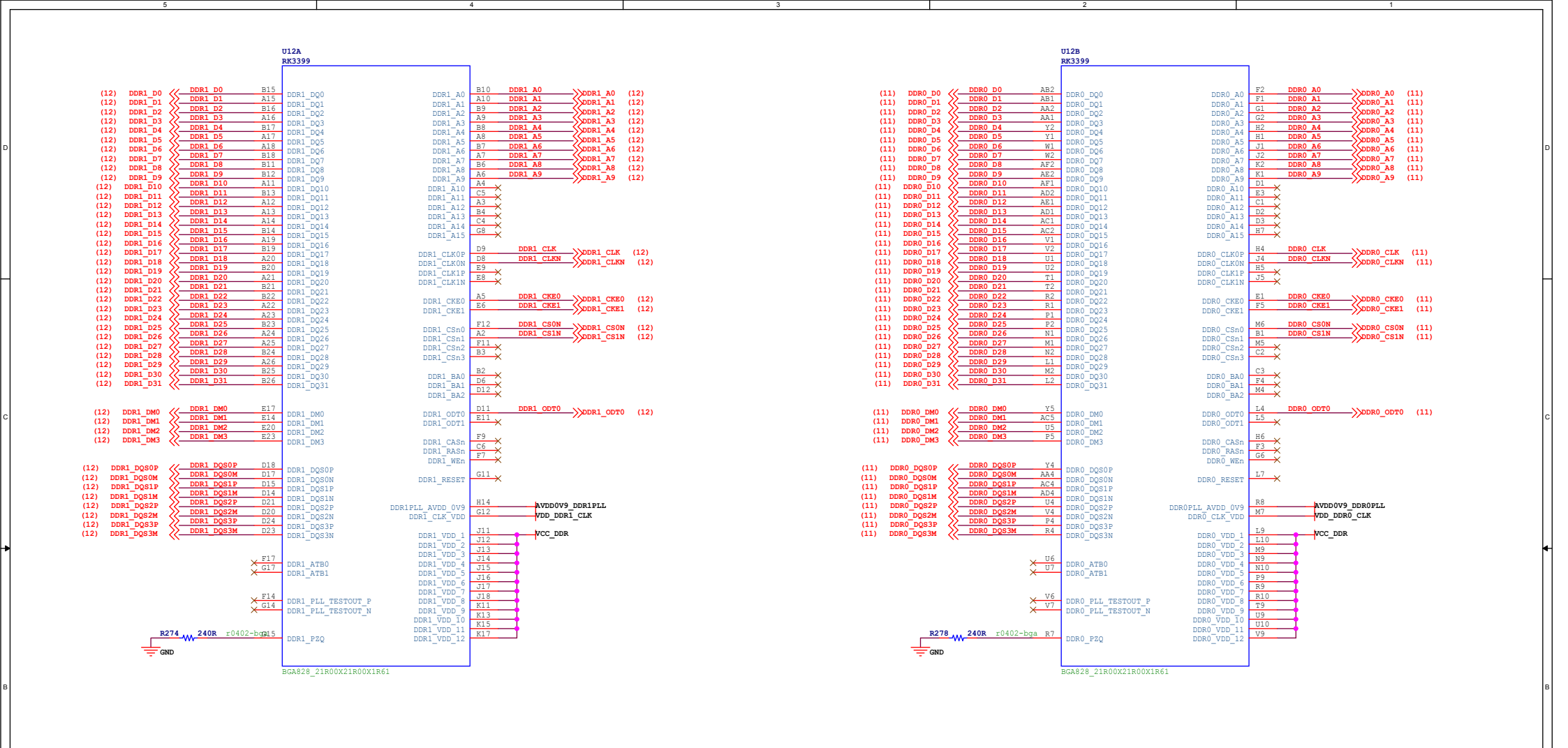




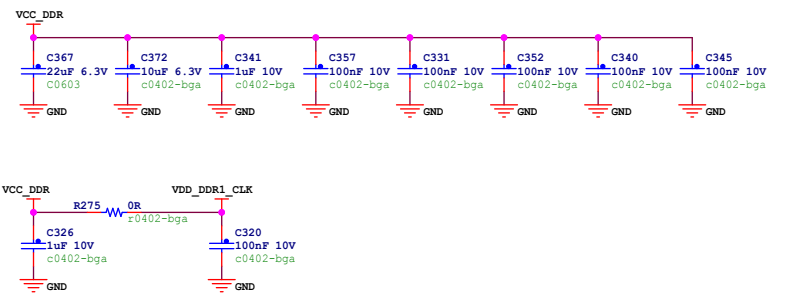
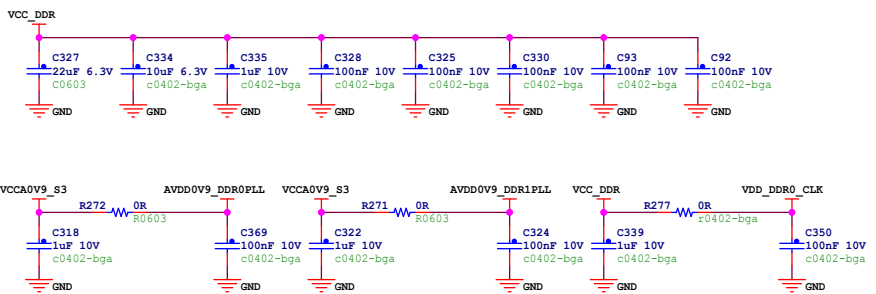
# TYPE-C INTERFACE



Vivid Unit V1.3		Dun Cat B.V.(UGGear)	
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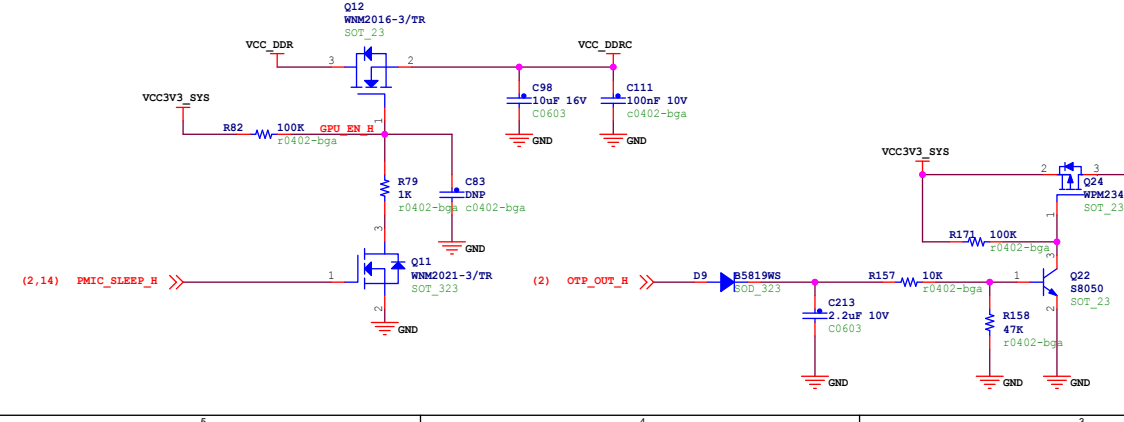
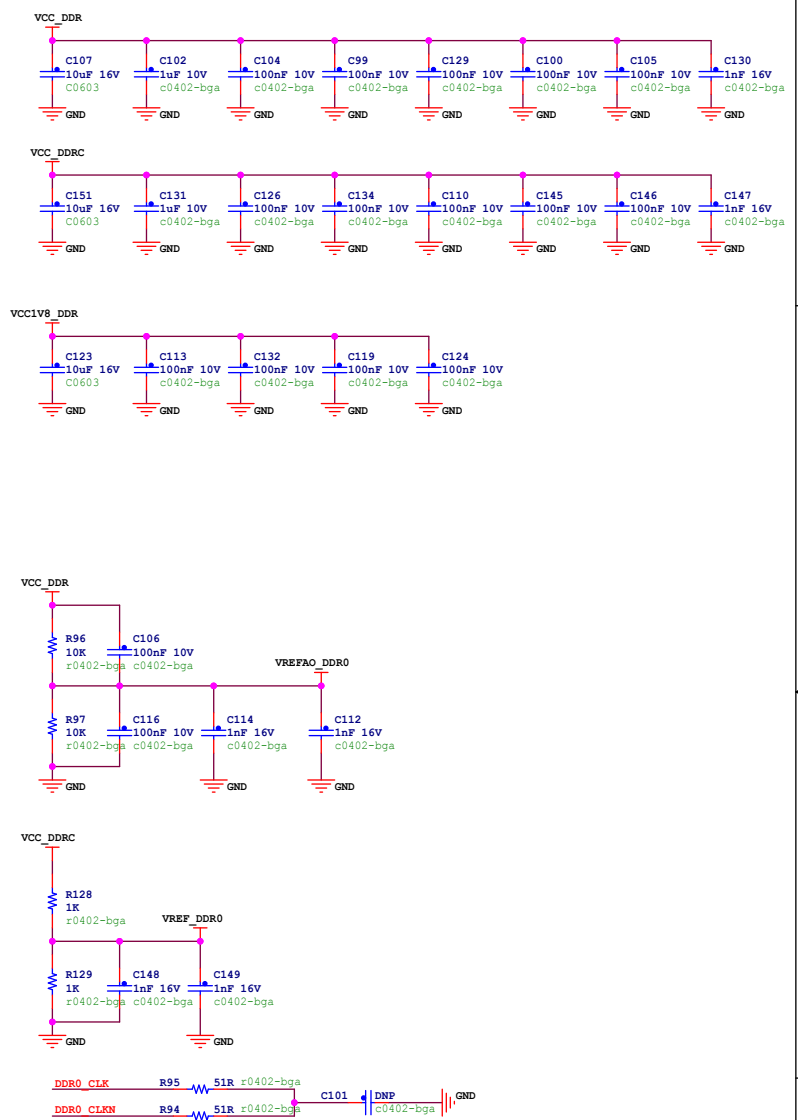
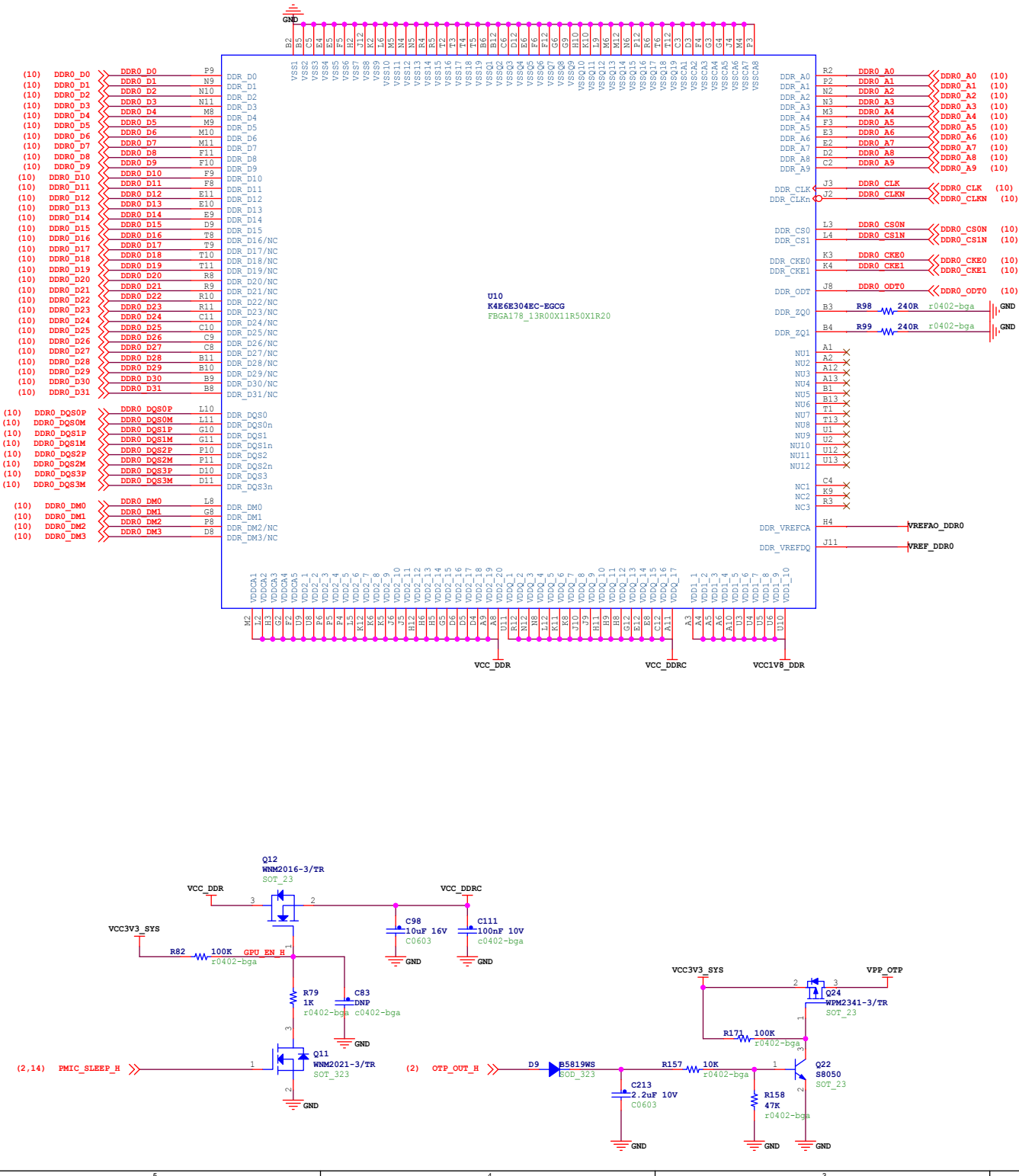


DDR FILTER



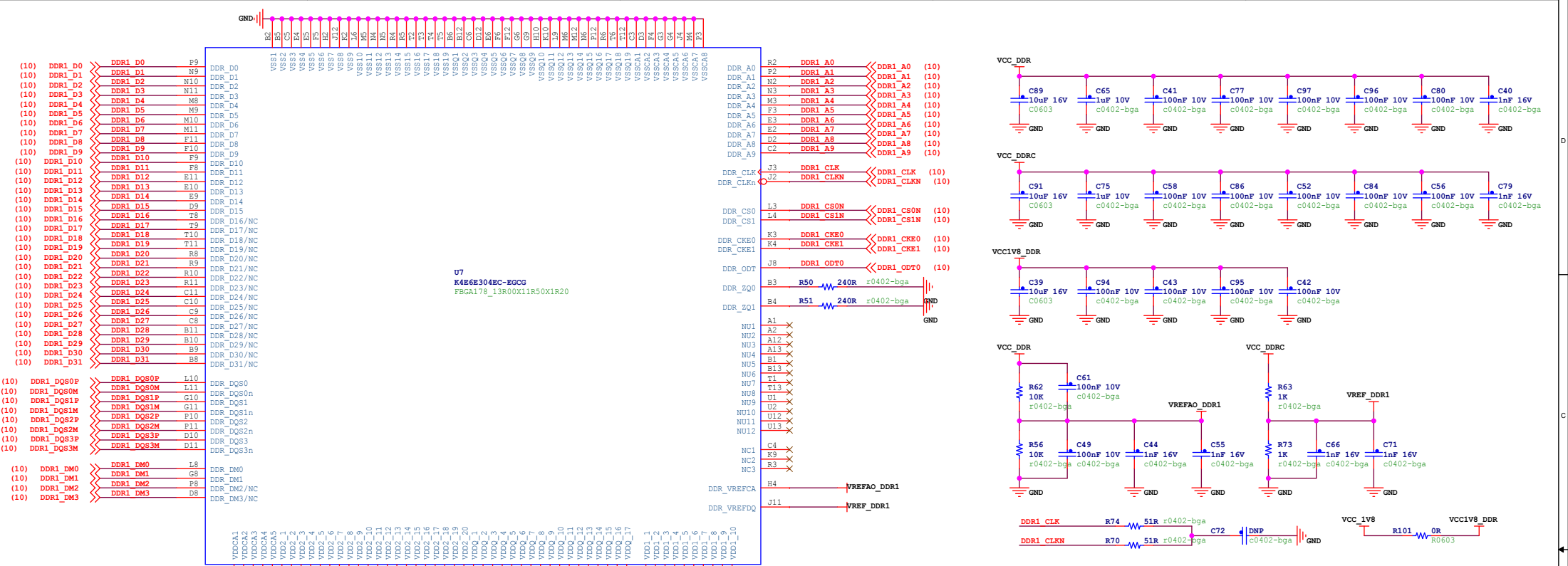
Vivid Unit V1.3		Dun Cat B.V.(UGear)	
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RK3399 DDR

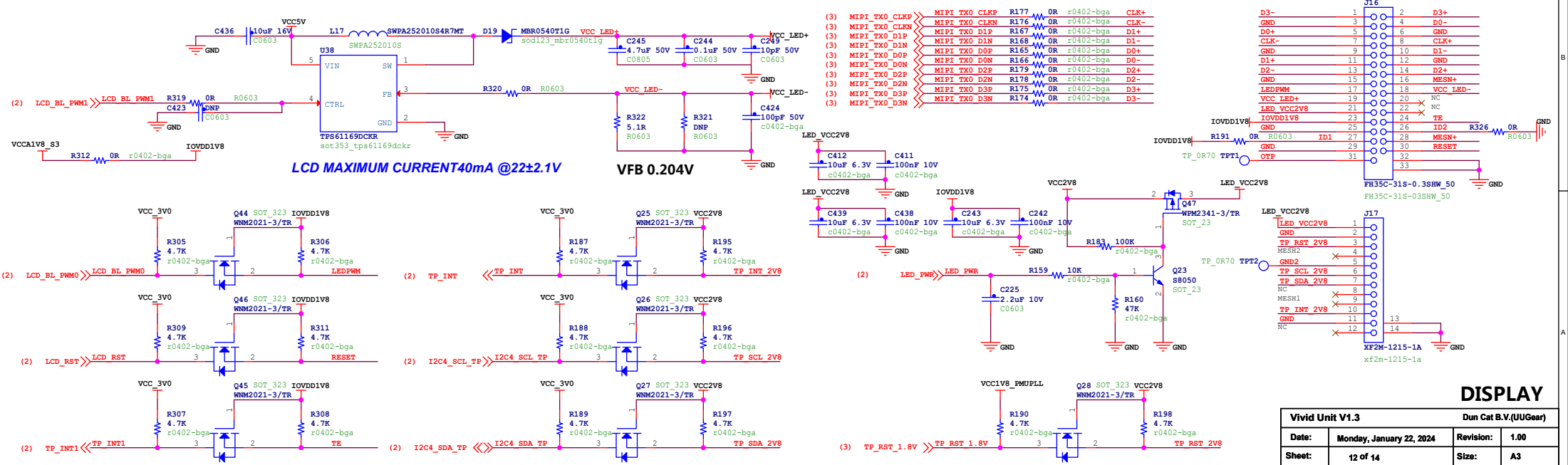


**RK3399 DDR3-1**

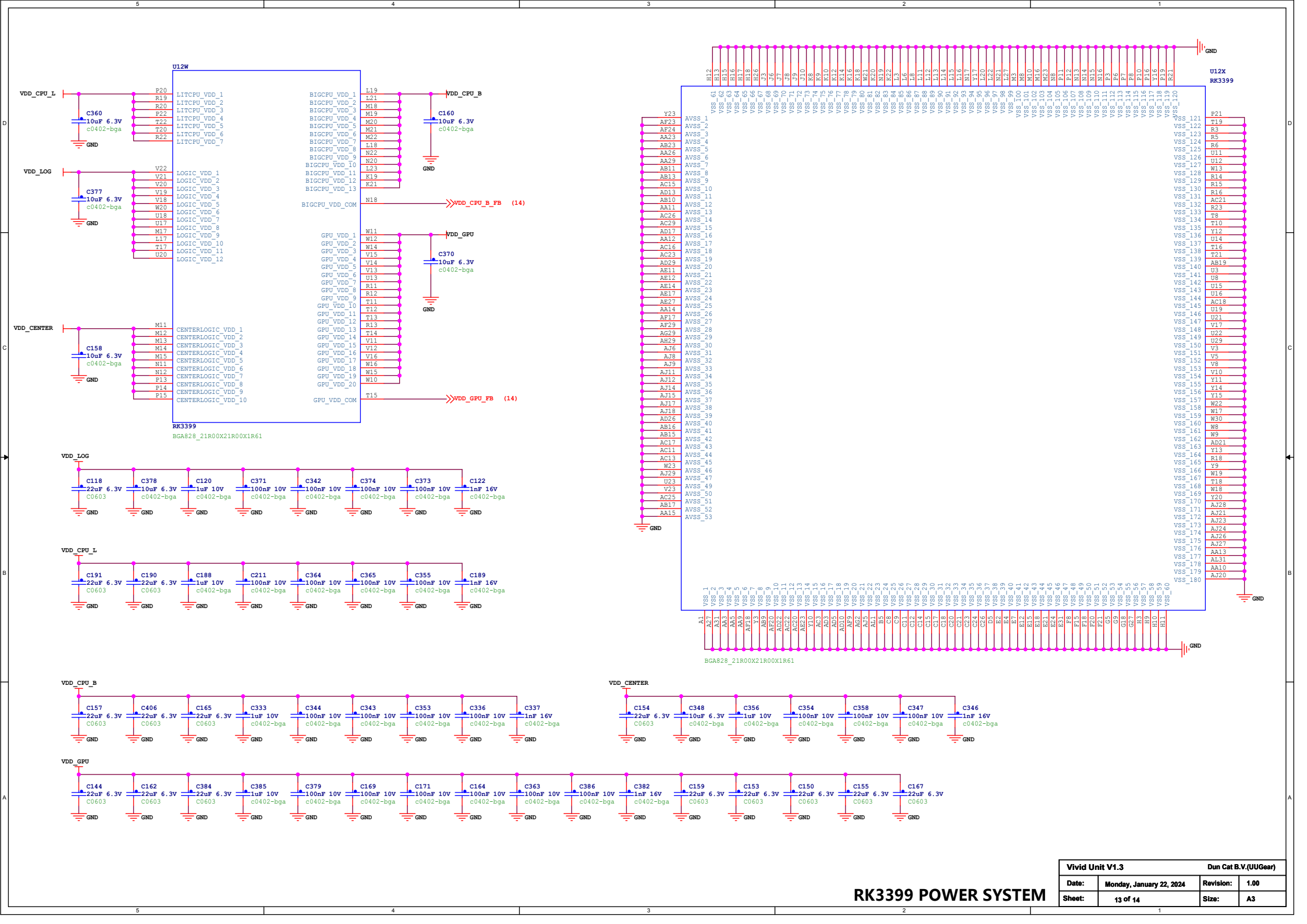
Vivid Unit V1.3		Dun Cat B.V.(UGGear)	
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## RK3399 DDR3-2



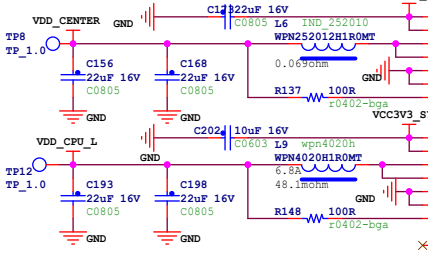
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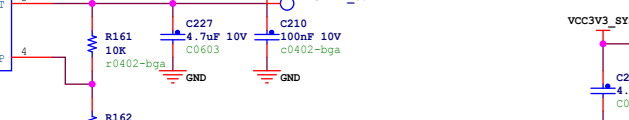
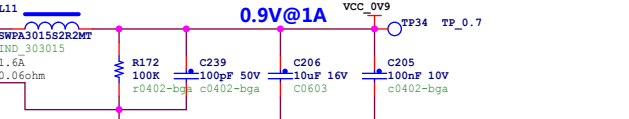
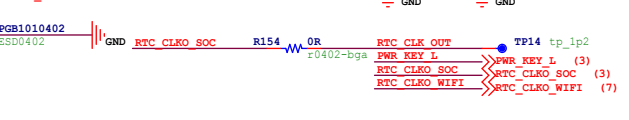
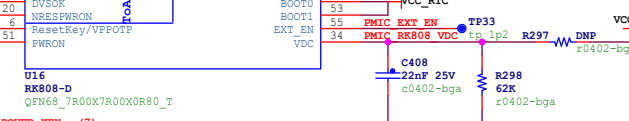
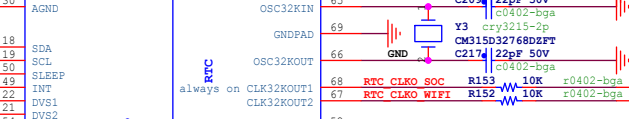
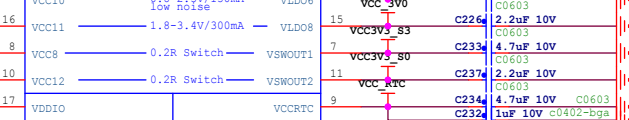
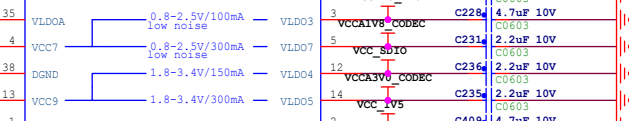
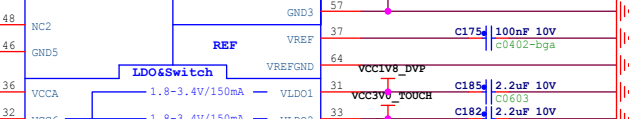
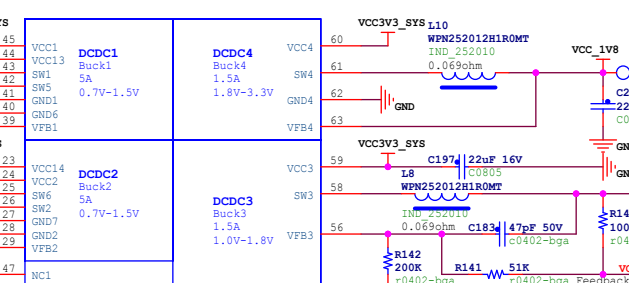
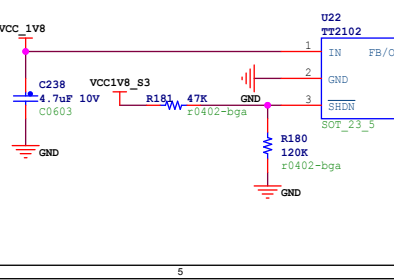
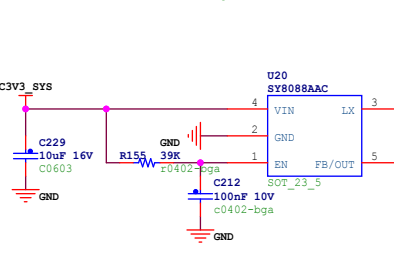
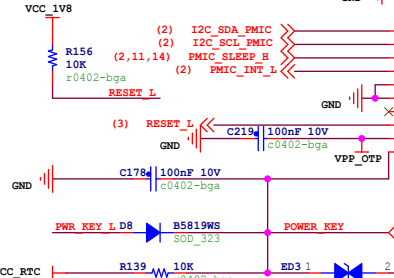
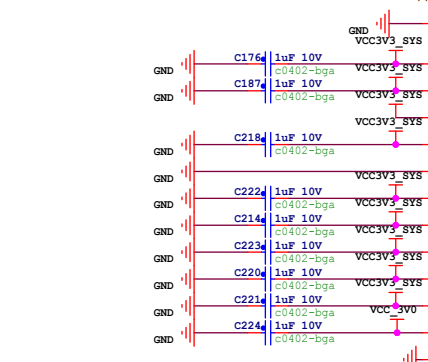
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**RK3399 POWER SYSTEM**

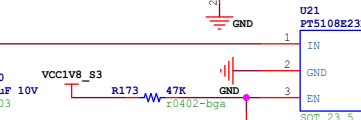
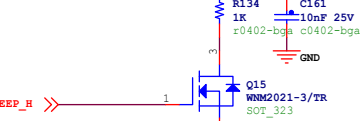
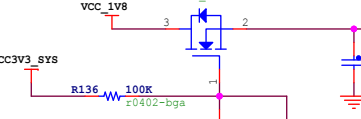
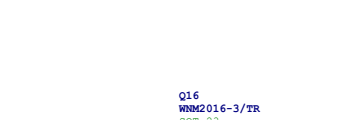
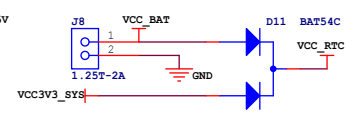
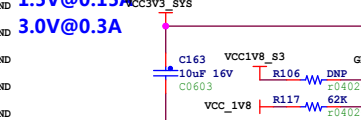
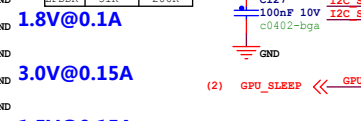
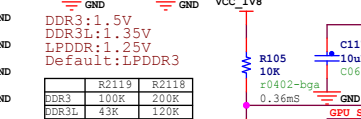
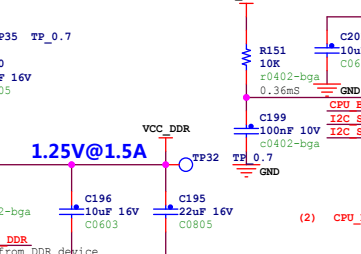
0.9V@5A



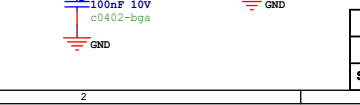
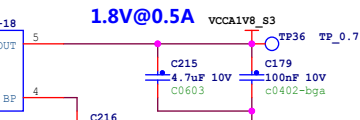
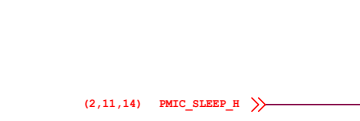
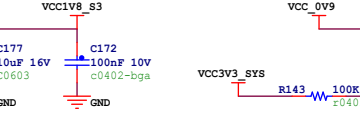
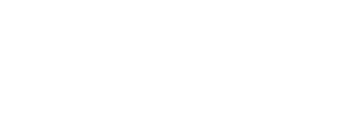
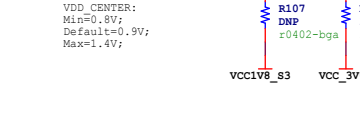
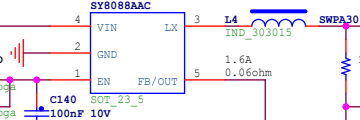
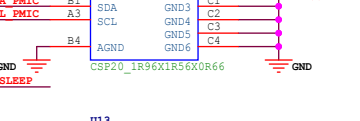
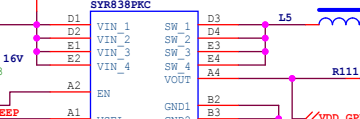
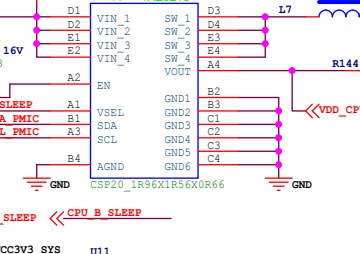
0.9V@5A



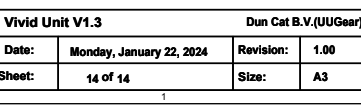
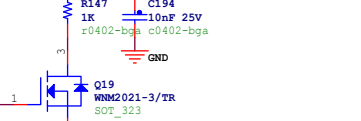
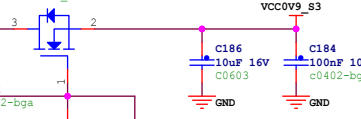
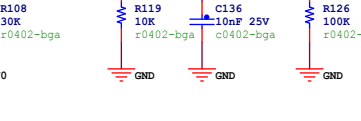
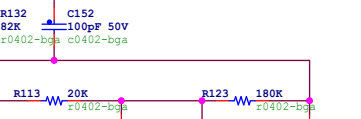
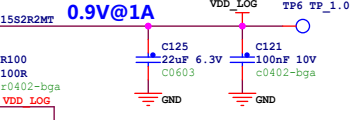
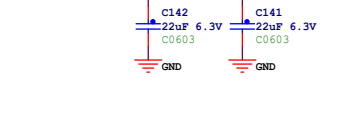
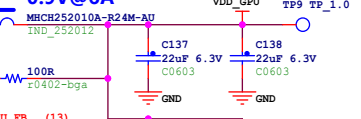
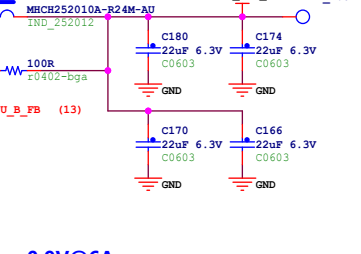
1.8V@1.5A



0.9V@6A



0.9V@6A



DDR3: 1.5V
DDR3L: 1.35V
LPDDR: 1.25V
Default: LPDDR3
DDR3: 100K 200K
DDR3L: 43K 120K
LPDDR: 51K 200K

1.8V@0.1A

3.0V@0.15A

1.5V@0.15A

3.0V@0.3A

0.9V@1A

0.9V@1A

0.9V@1A

0.9V@1A

0.9V@1A

0.9V@1A

0.9V@1A

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RK3399 PMIC

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